

# Influence of body and BOX thicknesses on the digital performance of FDSOI devices

Alex G. Reimberg  
 Electrical Engineering Department  
 Centro Universitário FEI  
 São Bernardo do Campo, Brazil  
 alex.reimberg@outlook.com

Natasha Merzbahcer  
 Electrical Engineering Department  
 Centro Universitário FEI  
 São Bernardo do Campo, Brazil  
 nacrismerzbahcer@fei.edu.br

Ariane S. N. Pereira  
 Electrical Engineering Department  
 Centro Universitário FEI  
 São Bernardo do Campo, Brazil  
 ariannesoes@fei.edu.br

**Abstract**— The aim of this work is to do a comparative analysis of threshold voltage, subthreshold slope and body factor of three SOI (Silicon-On-Insulator) technology structures: FDSOI, UTB and UTBB as a function of channel length and silicon film thickness. The analysis was based on results from bidimensional numerical simulation. The results shown that for  $L=100$  nm, the FDSOI structure started to suffer on short channel effects, while the UTB and UTBB devices started to degrade the subthreshold slope for  $L=30$ nm, showing that both the reduction of  $t_{Si}$  and  $t_{BOX}$  contribute to a better short channel response. In the analysis as a function of the silicon film thickness, the reduction of  $t_{Si}$ , brought the subthreshold slope close to the limit, with a decrease from 88mV/dec to 62mV/dec in S by reducing 23nm in  $t_{Si}$ .

**Keywords** — SOI devices, threshold voltage, subthreshold slope, body factor, short channel effects.

## I. INTRODUCTION

SOI (Silicon-On-Insulator) technology emerged from the requirement of reduced dimensions of MOS (Metal-Oxide-Semiconductor) devices. This technology presents a buried oxide (BOX), that isolates the active region of the transistor from the substrate, reducing the influence of source and drain depletion in the channel region, recovering part of the gate control of channel charges [1].

The SOI technology evolved from FDSOI (Fully-Depleted SOI), with a thin silicon layer, to UTB (Ultra-Thin Body) and then, to UTBB (Ultra-Thin Body and BOX). The silicon film thickness reduction allowed a better short-channel response. However, for technologic nodes below 100 nm, the ultra-thin body can suffer with the increase of the second interface potential induced by the BOX and, consequently, with SCE (Short Channel Effects). In this context, the reduction of BOX thickness was proposed [2] and, since then, UTBB has demonstrated that can reach the 8 nm node if the silicon film and the BOX thicknesses are scaled down to order of 5 nm and 10 nm, respectively [3].

This work intends to compare the digital performance of three SOI structures: FDSOI, UTB and UTBB. The figures of merit that will be used are: the threshold voltage ( $V_T$ ), the subthreshold slope (S) and the body factor ( $n$ ) [4]. These parameters were extracted from the simulated drain current as a function of gate voltage for different channel lengths and silicon film thicknesses.

## II. NUMERICAL SIMULATIONS

### A. Devices Characteristics

The SOI structure is presented in Fig.1, where  $t_{ox}$  is the gate oxide thickness,  $t_{Si}$  is the silicon film thickness,  $t_{BOX}$  is the buried oxide thickness and  $L$  is the channel length.

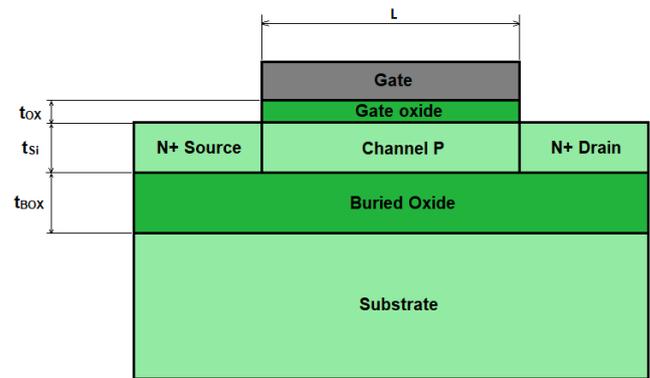


Fig. 1 – SOI structure.

The dimensional characteristics of the three simulated structures are presented in Table I. Notice that the UTB has the  $t_{Si}$  reduction compared to FDSOI and the UTBB has the  $t_{BOX}$  reduction compared to UTB.

TABLE I. SOI STRUCTURES CHARACTERISTICS

	$t_{ox}$ (nm)	$t_{Si}$ (nm)	$t_{BOX}$ (nm)
FDSOI	1.3	30	150
UTB	1.3	7	150
UTBB	1.3	7	25

The following characteristics are common to the three structures: channel lengths ( $L$ ) of 30, 50, 100, 200 and 500nm, p-type channel doping concentration ( $N_A$ ) of  $1 \times 10^{15} \text{cm}^{-3}$ , n-type source and drain doping concentration ( $N_D$ ) of  $1 \times 10^{20} \text{cm}^{-3}$ . Two-dimensional numerical simulations were performed using Silvaco Atlas device simulator [5], for room temperature and including the physical models of Klassen and Shirahata for mobility, SRH (Shockley-Read-Hall) for recombination of carriers, BGN for bandgap narrowing. All physical models were used with the default parameters as implemented in Atlas device simulator.

### B. Electrical Characteristics

The simulations were performed for a low drain bias ( $V_{DS}=50$  mV), substrate voltage  $V_{GB}=0$  and gate voltage  $V_{GS}$  varying from 0 up to 1 V.

Fig. 2 shows the  $I_{DS} \times V_{GS}$  curves for the different SOI structures and channel lengths of 100, 200 and 500nm. The drain current is presented in logarithmic scale, where is possible to observe the subthreshold regime, that indicates how sharply the transistor is turned off by the gate voltage [4]. In FDSOI device a degradation in slope is noticed for the shorter channel length, which will be discussed in results section.

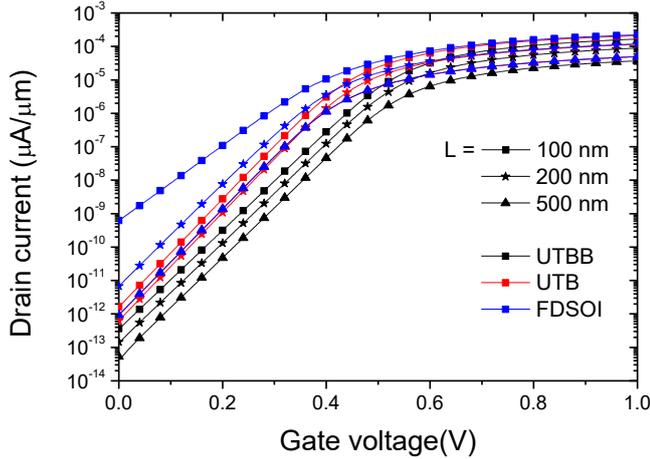


Fig. 2 – Drain current as a function of gate voltage for the different SOI structures and channel lengths of 100, 200 and 500nm.

### III. RESULTS AND DISCUSSION

The results analysis will be separated as a function of two dimensional parameters: channel length ( $L$ ) and silicon film thickness ( $t_{Si}$ ) as follows.

#### A. Analysis as a function of channel length ( $L$ )

Fig. 3 shows the threshold voltage ( $V_T$ ) as a function of channel length. The  $V_T$  values were extracted using the transconductance derivative method [6]. The threshold voltage is a technology dependent parameter, so, for the same technology, the values are expected to be constant with channel length.

A reduction in  $V_T$  can be observed for FDSOI structure with for  $L=100$ nm, which indicates that the device is suffering from short channel effects (SCE) [1], while the UTB and UTBB devices kept the same  $V_T$  values for this channel length. In other words, both the reduction of  $t_{Si}$  and  $t_{BOX}$  contributed to a better short channel response.

The UTB and UTBB have a small reduction in the threshold voltage for the channel length of 30nm, which will be better investigated with the results for subthreshold slope and body factor.

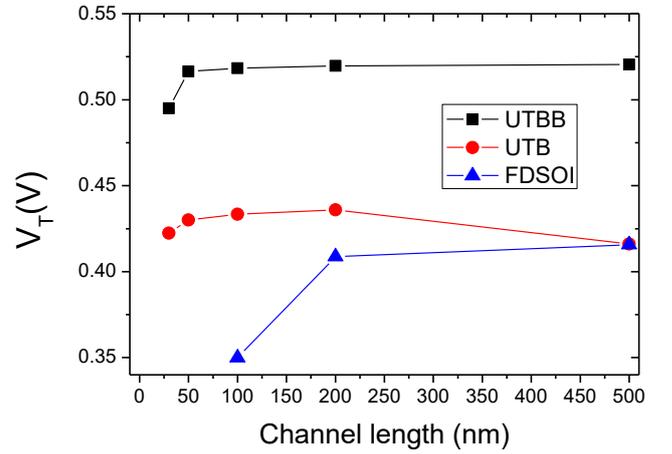


Fig. 3 – Threshold voltage as a function of channel length for FDSOI, UTB and UTBB.

The SCE can be better understood by the analysis of Fig. 4 [1], that represents the influence of source and drain depletion “ $d$ ” in the channel region of long-channel (left) and short-channel (right) devices. Notice that the “ $d$ ” influence become significantly with  $L$  reduction, contributing to increase the inversion charge, hence, reducing  $V_T$ . Thanks to  $t_{Si}$  reduction, for  $L=100$  nm in Fig. 3, the  $V_T$  of the UTB device is kept the same of long ones, due to the “ $d$ ” influence is reduced in this case.

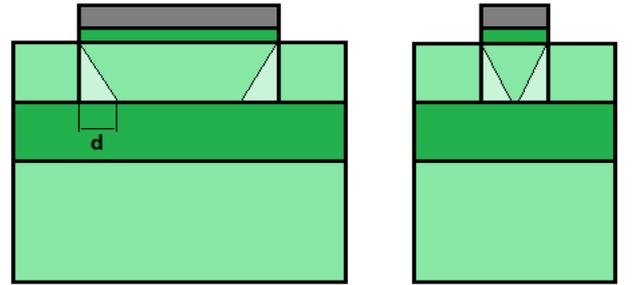


Fig. 4 – Influence of source and drain depletion “ $d$ ” in long-channel (left) and short-channel (right) SOI devices [1].

The subthreshold slope ( $S$ ) was also analyzed. The values were extracted from the curves presented in Fig. 2 using the definition of the inverse of current variation with the gate voltage in subthreshold region, as shown in equation (1) [4]:

$$S = \frac{dV_G}{d(\log I_{DS})} \quad (1)$$

The  $S$  results as a function of channel length for  $L$  of 100, 200 and 500nm are presented in Fig. 5. The theoretical limit for  $S$  at room temperature is 60 mV/déc [4]. Notice that the UTB technology presented values close to the theoretical ones. For the longest channel, the UTBB technology presented the highest value, however, it kept constant for all the simulated channel lengths, while the FDSOI technology has a good result for  $L = 500$ nm and significantly degrades for  $L=100$ nm.

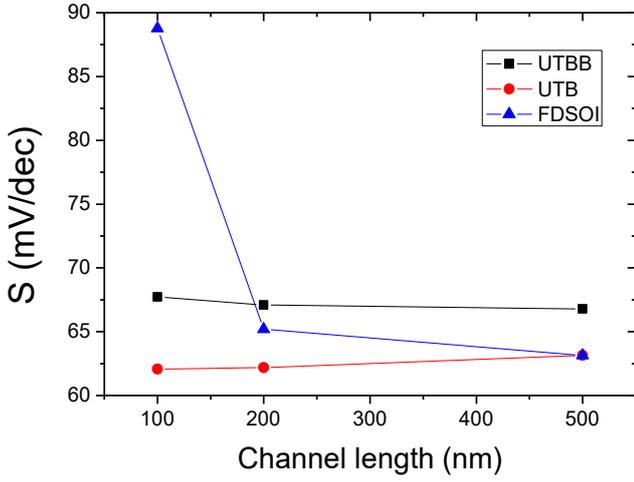


Fig. 5 – Subthreshold slope as a function of channel length for FDSOI, UTB and UTBB.

The body factor ( $n$ ) represents the coupling between the interfaces of the transistor. It is described by the association of capacitances between the gate and substrate terminals. Its ideal value is the unit and it is dimensionless.

The  $n$  values were extracted from  $S$ , which can be also defined in terms of body factor, as shown in equation (2) [7]:

$$S = \frac{k \cdot T}{q} \cdot \ln(10) \cdot n \quad (2)$$

where the term  $(k \cdot T/q)$  is the thermal potential.

There are models in literature for body factor depending on the structure. For a FDSOI with the second interface in depletion, the  $n$  can be calculated by equation (3) [1]:

$$n_{FD} = 1 + \frac{\epsilon_{Si} \cdot \frac{\epsilon_{OX}}{t_{BOX}}}{\epsilon_{OX} \left( t_{Si} \cdot \frac{\epsilon_{OX}}{t_{BOX}} + \epsilon_{Si} \right)} \quad (3)$$

where  $\epsilon_{Si}$  and  $\epsilon_{OX}$  are the electrical permittivity of, respectively, silicon and oxide.

For a UTBB device, the body factor is calculated by equation (4) [8]:

$$n_{UTBB} = 1 + \frac{t_{OX} + \frac{\epsilon_{OX}}{\epsilon_{Si}} \cdot \frac{t_{Si}}{2}}{t_{BOX} + \frac{\epsilon_{OX}}{\epsilon_{Si}} \cdot \frac{t_{Si}}{2}} \quad (4)$$

Fig. 6 presents the body factor extracted from simulations (symbols) and calculated from models (lines). It can be observed that FDSOI and UTB structures, have the better coupling. However, for the studied  $L$  range, the UTB has the best results for the shorter lengths. The value for

FDSOI structure with  $L=100$  nm presented extracted body factor of 1.5, for this reason it was suppressed in figure.

In equations (3) and (4) we can observe that the theoretical body factor have dependency only with the layers thicknesses the electrical permittivity of materials, for this reason the model curves show always constant values as a function of channel length. But, when the devices start to suffer with SCE, the models cannot predict such effect.

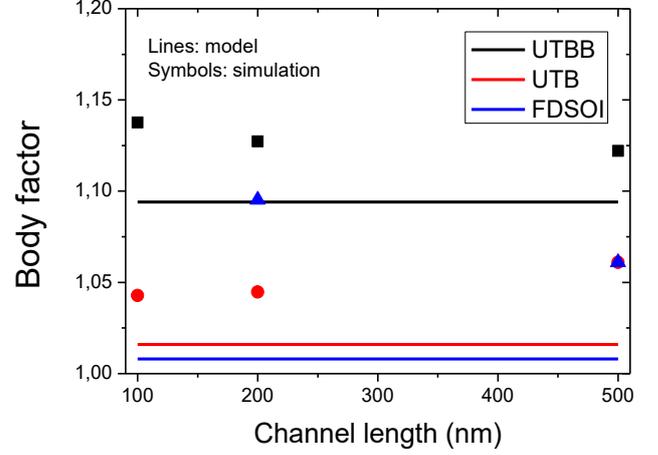


Fig. 6 – Body factor as a function of channel length for FDSOI, UTB and UTBB.

In order to analyze the UTB and UTBB behavior, a second analysis for smaller channel lengths, including 30 and 50nm, was made. Fig. 7 presents the subthreshold slope and body factor results for the channel lengths of 30, 50 and 100 nm. For both structures, there are a small degradation for  $L=50$ nm and a significant degradation for  $L=30$ nm. Notice that the variation is slightly small in UTBB. From the results, we can notice that the UTBB structure do not have the best coupling. Though, for technologic nodes below 20nm, such structure can work and attend short channel criterion [3].

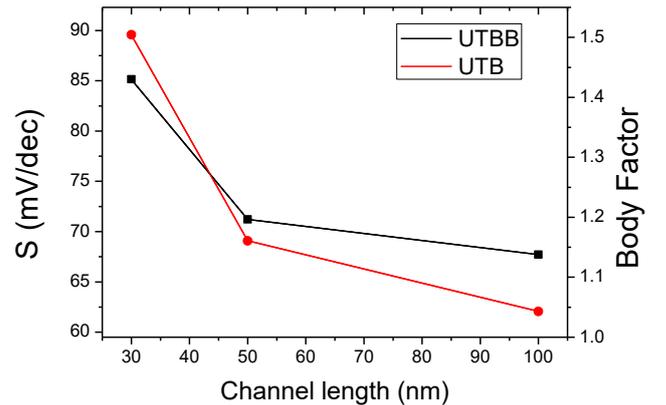


Fig. 7 – Subthreshold slope and body factor as a function of channel length for UTB and UTBB structures for the smaller channel lengths.

Table II summarizes the  $S$  values for the studied structures. Even for the shorter length, the UTB and UTBB presented reasonable  $S$  values, showing that, for the analyzed characteristics, both structures can attend the 30nm node.

TABLE II. SUBTHRESHOLD SLOPE OF THE THREE SOI STRUCTURES

Channel (nm)	UTBB	UTB	FDSOI
30	85,12	89,54	545,97
50	71,21	69,09	258,45
100	67,72	62,07	88,78
200	67,10	62,19	65,19
500	66,79	63,15	63,15

B. Analysis as a function of silicon film thickness ( $t_{Si}$ )

The purpose of this section is to observe how the  $t_{Si}$  reduction can reduce SCE. So, the case of  $L=100$  nm was taken and new simulations were performed for silicon film thicknesses of 10 and 20 nm, besides the 7nm and 30 nm points already presented, respectively, as UTB and FDSOI.

The results for subthreshold slope and body factor as a function of silicon film thickness are presented in Fig. 8. Notice that the reduction of  $t_{Si}$ , in fact, can bring the parameters to acceptable range in terms of short channel criterion. As a future work, the analysis will be extended as a function of BOX thickness and for lower channel lengths.

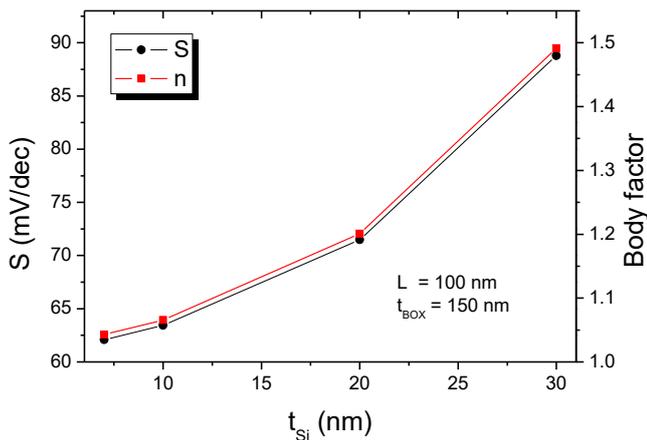


Fig. 8 – Subthreshold slope and body factor as a function of  $t_{Si}$  for thick BOX and short channel.

IV. CONCLUSIONS

This study analyzed the influence of channel length and silicon film thickness on the digital performance of FDSOI, UTB and UTBB devices. The used figures of merit was the threshold voltage, the subthreshold slope and the body factor.

In the analysis as a function of channel length, the influence of the SCE in FDSOI structure was observed for

$L=100$ nm, while the UTB and UTBB devices degrades from  $L=30$ nm, showing that both the reduction of  $t_{Si}$  and  $t_{BOX}$  contributed to a better short channel response.

Regarding to body factor, the long FDSOI and UTB structures have the better coupling, as predicted by models. The UTB and UTBB presented a small degradation for  $L=50$ nm and a significant degradation for  $L=30$ nm, but the variation is slightly small in UTBB.

In the analysis as a function of silicon film thickness, the reduction of  $t_{Si}$ , in fact, can bring the parameters to acceptable range in terms of short channel criterion, with a decrease from 88mV/dec to 62mV/dec in S by reducing 23nm in  $t_{Si}$ . As a future work, the analysis will be extended as a function of BOX thickness and for lower channel lengths.

ACKNOWLEDGMENT

Alex G. Reimberg would like to thank Centro Universitário FEI for the scientific scholarship.

REFERENCES

- [1] J. P. Colinge, Silicon-On-Insulator Technology: Materials to VLSI. 3rd ed., Boston: Kluwer academic, 2004.
- [2] T.Ernst, C.Tinella, C.Raynaud and S.Cristoloveanu, “Fringing fields in sub-0.1 um fully depleted SOI MOSFETs: optimization of the device architecture”. Solid-State Electronics, St. Louis, v. 46, pp. 373-378, March 2002.
- [3] O. Faynot, F. Andrieu, O. Weber, C. Fenouillet-Béranger, P. Perreau, J. Mazurier et al, “Planar fully depleted SOI technology: a powerful architecture for the 20nm node and beyond. IEEE International Electron Devices Meeting (IEDM), pp. 321–4, 2010.
- [4] S. M. Sze, Physics of Semiconductor Devices. New York: John Wiley & Sons, 1981.
- [5] ATLAS USER’s Manual, Version 5.19.20 R, 2010.
- [6] H. S. Wong et al. “Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET’s”. Solid-State Electronics, St. Louis, v. 30, pp. 953-968, 1987.
- [7] J. R. Brews, “Subthreshold behavior of uniformly and nonuniformly doped longchannel MOSFET”. IEEE Transactions on Electron Devices, Piscataway, v. 26, pp. 1282-1291, October 1979.
- [8] J.-P. Noel et al. “Multi-VT UTBB FDSOI device architectures for low-power CMOS circuit”. IEEE Transactions on Electron Devices, Piscataway, v. 58, pp. 2473-2482, August 2011.